\*\*\* SPICE deck for cell EmptyBufWLoad{lay} from library EE307W09

\*\*\* Created on Sat Jan 03, 2009 14:44:17

\*\*\* Last revised on Thu Dec 30, 2010 14:08:04

\*\*\* Written on Tue Jan 13, 2009 22:36:44 by Electric VLSI Design System,

\*version 8.08

\*\*\* Layout tech: mocmos, foundry MOSIS

\*\*\* UC SPICE \*\*\* , MIN\_RESIST 4.0, MIN\_CAPAC 0.1FF

\*\*\* P-Active: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* N-Active: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=3.0ohms/sq

\*\*\*

\*Polysilicon-1: areacap=0.1467FF/um^2, edgecap=0.0608FF/um, res=6.2ohms/sq

\*\*\* Polysilicon-2: areacap=1.0FF/um^2, edgecap=0.0FF/um, res=50.0ohms/sq

\*\*\* Transistor-Poly: areacap=0.09FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* Poly-Cut: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=2.2ohms/sq

\*\*\* Active-Cut: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* Metal-1: areacap=0.1209FF/um^2, edgecap=0.1104FF/um, res=0.078ohms/sq

\*\*\* Via1: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sq

\*\*\* Metal-2: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via2: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.9ohms/sq

\*\*\* Metal-3: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via3: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq

\*\*\* Metal-4: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* SPICE deck for cell EmptyBufWLoad{lay} from library EE307W13

\*\*\* Created on Sat Jan 03, 2009 14:44:17

\*\*\* Last revised on Sat Jan 12, 2013 17:22:16

\*\*\* Written on Tue Jan 13, 2009 22:36:44 by Electric VLSI Design System,

\*version 8.08

\*\*\* Layout tech: mocmos, foundry MOSIS

\*\*\* UC SPICE \*\*\* , MIN\_RESIST 4.0, MIN\_CAPAC 0.1FF

\*\*\* P-Active: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* N-Active: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=3.0ohms/sq

\*\*\*

\*Polysilicon-1: areacap=0.1467FF/um^2, edgecap=0.0608FF/um, res=6.2ohms/sq

\*\*\* Polysilicon-2: areacap=1.0FF/um^2, edgecap=0.0FF/um, res=50.0ohms/sq

\*\*\* Transistor-Poly: areacap=0.09FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* Poly-Cut: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=2.2ohms/sq

\*\*\* Active-Cut: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq

\*\*\* Metal-1: areacap=0.1209FF/um^2, edgecap=0.1104FF/um, res=0.078ohms/sq

\*\*\* Via1: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sq

\*\*\* Metal-2: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via2: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.9ohms/sq

\*\*\* Metal-3: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via3: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq

\*\*\* Metal-4: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via4: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq

\*\*\* Metal-5: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq

\*\*\* Via5: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq

\*\*\* Metal-6: areacap=0.0423FF/um^2, edgecap=0.1273FF/um, res=0.036ohms/sq

\*.OPTIONS NOMOD NOPAGE

\*\*\* CELL: EE307W13:EmptyBuffer{lay}

.SUBCKT EmptyBuffer In Out gnd vdd

\*\* Extracted Parasitic Capacitors \*\*\*

MN1 3 In gnd gnd CMOSN L=0.4u W=2u

\*L=0.4u W=2.64u

MP1 3 In vdd vdd CMOSP L=0.4u W=8u

\*L=0.4u W=10.56u

MN2 Out 3 gnd gnd CMOSN L=0.4u W=5u

\*L=0.4u W=5.26u

MP2 Out 3 vdd vdd CMOSP L=0.4u W=20u

\*L=0.4u W=21.12u

\* D G S B

\*

\* Electric didn't produce the code between \*1 and \*2

\* Braun added it as an example

\*2

\*\* Extracted Parasitic Resistors \*\*\*

.ENDS EmptyBuffer

\*\*\* CELL: EE307W13:InvLoad{lay}

.SUBCKT InvLoad In Out gnd vdd

Mnmos-10 gnd In\_1nmos-10\_n-trans-poly-left Out gnd CMOSN L=0.4U W=0.8U AS=1.4P

+AD=2.32P PS=5U PD=8.8U

Mpmos-5 Out In\_2pmos-5\_p-trans-poly-right vdd vdd CMOSP L=0.4U W=0.8U AS=2.9P

+AD=1.4P PS=11U PD=5U

\*\* Extracted Parasitic Capacitors \*\*\*

C0 Out 0 3.667fF

C1 In 0 1.039fF

\*\* Extracted Parasitic Resistors \*\*\*

R0 In\_1nmos-10\_n-trans-poly-left In\_1nmos-10\_n-trans-poly-left\_\_0 9.3

R1 In\_1nmos-10\_n-trans-poly-left\_\_0 In\_1nmos-10\_n-trans-poly-left\_\_1 9.3

R2 In\_1nmos-10\_n-trans-poly-left\_\_1 In\_1nmos-10\_n-trans-poly-left\_\_2 9.3

R3 In\_1nmos-10\_n-trans-poly-left\_\_2 In\_1nmos-10\_n-trans-poly-left\_\_3 9.3

R4 In\_1nmos-10\_n-trans-poly-left\_\_3 In 9.3

R5 In In\_\_0 9.817

R6 In\_\_0 In\_\_1 9.817

R7 In\_\_1 In\_\_2 9.817

R8 In\_\_2 In\_\_3 9.817

R9 In\_\_3 In\_\_4 9.817

R10 In\_\_4 In\_2pmos-5\_p-trans-poly-right 9.817

.ENDS InvLoad

\*\*\* TOP LEVEL CELL: EmptyBufWLoad{lay}

XBufOut In Out 0 vdd InvLoad

XIn In\_In In 0 vdd EmptyBuffer

\*\* Extracted Parasitic Capacitors \*\*\*

C0 In 0 0.411fF

\*\* Extracted Parasitic Resistors \*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\* \*

\* The above circuit file results after substituting \*

\* "\_" for "#" \*

\* "-" for "@" \*

\* NMOS model name "CMOSN" for "N" \*

\* PMOS model name "CMOSP" for "P" \*

\* \*

\* In the TOP LEVEL CELL, substitute node "0" for "gnd" \*

\* \*

\* The above file also comments out the ".OPTIONS NOMOD NOPAGE" line \*

\* \*

\* Electric didn't produce the rest of the file \*

\* \*

\* Remember to add the transistor models and load capacitance Cout \*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Cout In 0 1.2p

Vdd vdd 0 5

Vin In\_In 0 PULSE (0 5 0 5p 5p 49.5n .1u)

\*.DC Vin 0 5 0.01

.TRAN .1n .5u 0 .1n

.PROBE

.OP

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\* FET Model Parameters \*

\* From http://www.mosis.org/Technical/Testdata/t14y\_tsmc\_025\_level3.txt \*

\* TSMC (0.25 micron) DATE: Jun 11/01 LOT: T14Y WAF: 03 DIE: N\_Area\_Fring \*

\* DEV: N3740/10 \* Temp= 27 \*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.MODEL CMOSN NMOS ( LEVEL = 3

+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.4317311

+ PHI = 0.7 VTO = 0.442 DELTA = 0

+ UO = 425.6466519 ETA = 0 THETA = 0.1754054

+ KP = 6.501048E-4 VMAX = 8.287851E4 KAPPA = 0.1686779

+ RSH = 4.062439E-3 NFS = 1E12 TPG = 1

+ XJ = 3E-7 LD = 3.162278E-11 WD = 1.232881E-8

+ CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO = 1E-10

+ CJ = 1.81211E-3 PB = 0.5 MJ = 0.3282553

+ CJSW = 5.341337E-10 MJSW = 0.5 )

.MODEL CMOSP PMOS ( LEVEL = 3

+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.6348369

+ PHI = 0.7 VTO = -0.542 DELTA = 0

+ UO = 250 ETA = 0 THETA = 0.1573195

+ KP = 1.619415E-4 VMAX = 2.295325E5 KAPPA = 0.7448494

+ RSH = 30.0776952 NFS = 1E12 TPG = -1

+ XJ = 2E-7 LD = 9.968346E-13 WD = 5.475113E-9

+ CGDO = 6.66E-10 CGSO = 6.66E-10 CGBO = 1E-10

+ CJ = 1.893569E-3 PB = 0.9906013 MJ = 0.4664287

+ CJSW = 3.625544E-10 MJSW = 0.5 )

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.END